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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/001,477	11/01/2001	Steve Roe	CYPR-CD01203M	6440

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EXAMINER	
PROCTOR, JASON SCOTT	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 03/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/001,477	ROE ET AL.	
	Examiner	Art Unit	
	Jason Proctor	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14 and 17-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 17-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 1/13/06
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12 December 2005 has been entered.

Claims 1-20 were rejected in Office Action of 24 October 2005. In response, claim 14 has been amended, claims 15-16 have been cancelled, and claims 1-14 and 17-20 have been submitted for reconsideration.

Claims 1-14 and 17-20 have been rejected.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 13 January 2006 was filed after the mailing date of the Final Rejection on 24 October 2005. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Priority

2. This Application contains a claim for the benefit of priority to U.S. Provisional Application No. 60/243,708 filed 26 October 2000. The provisional application has been reviewed and priority is denied, because the provisional application does not appear to enable the claimed invention as required under 35 U.S.C. Section 112, first paragraph. See 35 U.S.C. § 119(e)(1).

For example, the provisional application contains a set of 'powerpoint-style' drawings and datasheets describing desired features for a microcontroller or a 'system-on-chip,' but this material does not appear to contain either the text description or the drawings found in the Application. In particular, no part of the provisional application appears to disclose the method steps shown in the Application at Fig. 7.

Double Patenting

3. Claims 1, 7, and 14 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 13 of copending Application No. 09/975,338. Although the conflicting claims are not identical, they are not patentably distinct from each other because where the limitations of claim 13 of the copending application only differ semantically from the independent claims 1, 7, and 14 of the instant application. Where claims from copending applications cover the same subject matter but are claimed slightly differently, it would have been obvious to a person of ordinary skill in the art to claim the invention in slightly different terms as exhibited the conflicting claims.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Applicants' response states that Applicants will correspond to the provisional double patenting rejection upon an indication of allowance of subject matter of either the present application or the co-pending application (09/975,338).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. § 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. § 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any

evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. § 103(c) and potential 35 U.S.C. § 102(e), (f) or (g) prior art under 35 U.S.C. § 103(a).

4. Claims 1-14 and 17-20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over US Patent No. 5,748,875 to Tzori (Tzori) in view of "Debugging with The GNU Source-Level Debugger" by Richard M. Stallman and Roland H. Pesch (Stallman).

Regarding claim 1, Tzori explicitly teaches a simulated (virtual) processor (column 8, lines 15-17) operating in lockstep with a second processor (column 8, lines 24-33; column 12, lines 11-19). The object of Tzori's system is to facilitate design and debugging of an integrated circuit (column 1, line 50 – column 2, line 4; column 4, lines 14-24). The method used by Tzori's system (Fig. 3; column 10, line 62 – column 12, line 19) is extremely applicable to the use of breakpoints by virtue of the stimulus-response method of execution. Tzori teaches that upon receiving data from the actual processor, the simulation process processes response data from the digital logic IC (column 12, lines 11-16). At this stage of the method, the simulated processor and actual processor have executed the same instructions; results from both are known and could be compared.

It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention that Tzori's system and method are readily adaptable to include standard, well-known debugging techniques such as the use of breakpoints. For example, many types of breakpoints require evaluations of logical expressions. To facilitate these types of breakpoints,

Tzori teaches processing the response data. Processing the response data to evaluate a logical expression, such as for a breakpoint, would be obvious to a person of ordinary skill in the art. Tzori teaches a system that facilitates debugging but leaves the particular details of the debugging open to methods known in the art.

Official notice is taken that the use of breakpoints, implemented by using a table of addresses and a flag to indicate the presence of a breakpoint at a given address is extremely well known in the art (See Stallman, "Setting breakpoints"). It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to use the breakpoint feature of a well-known debugger, such as the GNU Source-Level Debugger, often referred to as GDB, in combination with the system taught by Tzori to produce a complete emulation and debugging tool [*"Alternatively, even though an IC is available for use in implementing and testing a digital logic system's design, analogous to the use of an ICE in designing and debugging a digital logic system, a designer may want or need to observe and monitor the IC's interaction with other circuit elements, such as other ICs."* (Tzori, column 3, lines 35-49)]. The combination could be achieved by monitoring the results from the simulated and actual processor and setting breakpoints accordingly. Motivation to combine the references is expressly taught by Stallman [*"The principal purposes of using a debugger are so that you can stop your program before it terminates; or so that, if your program rums into trouble, you can investigate and find out why."* (page 1 of 13, "Stopping and Continuing")].

In response, Applicants argue primarily that:

> Applicants respectfully assert that Tzori fails to suggest, teach, or describe the limitations of "a virtual microcontroller operating in lock-step synchronization with the microcontroller" as recited in Claim 1.

> Specifically, as described in lines 1-8 of page 17 of the application as filed, the phrase "lock-step synchronization" should be understood as follows:
>
> > Synchronization between the microcontroller 232 and the virtual microcontroller 220 is achieved by virtue of their virtually identical operation. They are both started simultaneously by a power on or reset signal. They then track each other's operation continuously executing the same instructions using the same clocking signals. The system clock signal and the microcontroller clock signal are shared between the two microcontrollers (real and virtual) so that even if the microprocessor clock is changed during operation, they remain in lockstep.
>
> In contrast, Applicants understand Tzori to teach a digital logic simulator coupled to a hardware pod for carrying out stimulation-response cycles (Abstract; Figure 1).

The Examiner traverses this argument as follows.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the specific interpretation of "lock-step synchronization") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Applicants' arguments are directed toward what is understood as an exemplary embodiment of the invention and not the invention defined by the claims. If it is that embodiment for which Applicants seek patent protection, amending the claims to reflect that specific embodiment would improve the arguments presented above and may distinguish the claimed invention over the applied prior art.

Applicants further argue that:

> [...] Tzori fails to suggest, teach, or describe the limitations of "a break bit associated with each of a plurality of instruction addresses" and "the break bit being set to indicate that a break is to occur at a specified instruction address" as recited in Claim 1.

The Examiner traverses this argument as follows.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

In the rejection, the Stallman reference has been cited to teach these limitations.

Applicants further argue that:

> However, Stallman fails to suggest, teach, or describe the use of break bits associated with instruction addresses and stored in a breakpoint lookup table to effectuate an instruction break as claimed. Moreover, by teaching breakpoints without the use of break bits as claimed, Stallman effectively teaches away from the claimed embodiments.

The Examiner respectfully traverses this argument as follows.

As presented in the rejection, Stallman indeed suggests and teaches the limitations relating to break bits and a breakpoint lookup table, as was explicitly pointed out in the previous Office Action. See "info breakpoints [n], info break [n], info watchpoints [n]" on page 3 of 13. Stallman explicitly discloses that these commands *"Print a table of all breakpoints and watchpoints set and not deleted"*.

Applicants' allegation that Stallman "effectively teaches away from the claimed embodiments" is unpersuasive. "Furthermore, 'the prior art's mere disclosure of more than one alternative does not constitute a teaching away from any of these alternatives because such disclosure does not criticize, discredit, or otherwise discourage the solution claimed....' *In re Fulton*, 391 F.3d 1195, 1201, 73 USPQ2d 1141, 1146 (Fed. Cir. 2004)." See MPEP 2145.

Applicants further argue that:

> [...] Tzori teaches a digital logic simulator without the use of breakpoints, break bits, or the like.

The Examiner respectfully traverses this argument as follows.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

In the rejection, the Stallman reference has been cited to teach these limitations.

Applicants' further argue that:

> Consequently, Stallman also fails to suggest, teach, or describe the limitations of "a breakpoint controller that sends a break message to the microcontroller whenever an instruction address is encountered that is associated with a set break bit" as recited in Claim 1.

The Examiner respectfully traverses this argument as follows.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

In the rejection, the Tzori reference has been cited to teach the microcontroller arrangement, and the combination of references as set forth in the rejection teaches these limitations.

Applicants present analogous arguments for claim 14. Those arguments have been addressed above.

Applicants' arguments have been fully considered but have been found unpersuasive.

Regarding claim 2, Tzori teaches that a server process transmits control data over an interface to the actual processor (column 5, lines 1-13). When creating the combination formed in the rejection of claim 1, it would have been obvious to a person of ordinary skill in the art to issue a control statement such as a break message using the existing facilities for stimulation-control data.

Regarding claim 3, the well-known details of implementing breakpoints would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention. Official notice is taken that it is extremely well known to search a table of data for a particular data element of interest. This use of Official Notice has not been traversed and is therefore considered admitted prior art. See MPEP 2144.03.

Regarding claim 4, Tzori teaches a host computer that controls the simulation system (Fig. 1, reference 24; column 8, lines 9-24). When creating the combination formed in the rejection of claim 1, it would have been obvious to a person of ordinary skill in the art to configure the breakpoints using the existing digital computer of the simulation system.

Regarding claim 5, Tzori teaches a two phase cycle comprising a control phase and a data transfer phase (column 11, lines 14-20; column 11, line 66 – column 12, line 10).

Regarding claim 6, when creating the combination formed in the rejection of claim 1, it would have been obvious to a person of ordinary skill in the art to issue a control statement such as a break message using the existing facilities for stimulation-control data.

Claims 7 and 8 recite a method of establishing a breakpoint in a microcontroller that recites substantially the same limitations of claim 1 and is rejected for the same reasons given for claim 1. Methods for setting and issuing breakpoints are extremely well known in the prior art and, as indicated above, the claimed method does not distinguish itself from these well-known methods.

Claim 9 recites substantially the same limitations as claim 4 and is rejected for the same reasons given for claim 4.

Claim 10 recites substantially the same limitations as claim 3 and is rejected for the same reasons given for claim 3.

Claim 11 recites the basic concept of a breakpoint. The combination formed in the rejection of claims 1 and 7 would render the concept of a breakpoint obvious to a person of ordinary skill in the art at the time of Applicants' invention.

Claims 12-13 recite substantially the same limitations as claims 5-6 and are rejected for the same reasons given for claims 5-6.

Claim 14 recites substantially the same limitations as claim 11 and is rejected for the same reasons as claim 11. The steps of determining and programming recite the basic concept of a breakpoint and do not distinguish the claimed method from the prior art.

Claim 17 recites a limitation found in claim 1 and is rejected for the same reasons given for claim 1.

Claim 18 recites a method of establishing a breakpoint in a microcontroller that recites substantially the same limitations of claim 1 and is rejected for the same reasons given for claim 1. Methods for setting and issuing breakpoints are extremely well known in the prior art and, as indicated above, the claimed method does not distinguish itself from these well-known methods.

Claim 19 recites substantially the same limitations as claim 4 and is rejected for the same reasons given above for claim 4.

Claim 20 recites substantially the same limitations as claim 5 and is rejected for the same reasons given above for claim 5.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached at (571) 272-3753. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason Proctor
Examiner
Art Unit 2123

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Paul L. Rodriguez 2/24/06
Primary Examiner
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